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### (54) Semiconductor memory device and information processing system

(57) A semiconductor memory device capable of performing transfer operation best suited to applications. An address input circuit (1) receives an input address, and a readout circuit (2) sequentially reads, from m of a plurality of n banks (5-1, 5-2, ...5-n), where m ≤

n, data corresponding to one address input via the address input circuit (1) in an automatic manner. A data output circuit (3) outputs the data read by the readout circuit (2) from the m banks to the outside as collective data.

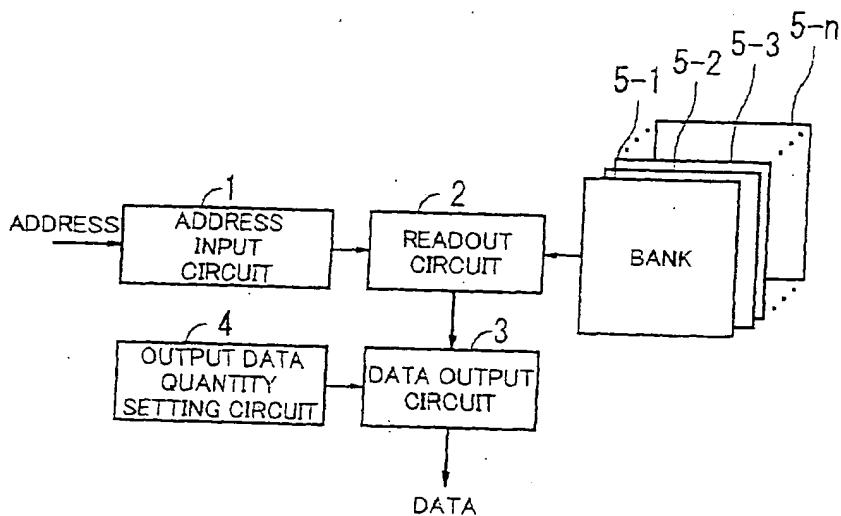


FIG. 1

**Description**

[0001] The present invention relates to a semiconductor memory device and an information processing system, and more particularly, to techniques of shortening the operation cycle time of a semiconductor memory device and an information processing system.

[0002] A semiconductor memory device and a control device for controlling the memory device exchange data with each other in blocks of bits whose number is determined, for example, by an application such as an OS (Operating System).

[0003] In the case of an application wherein the number of bits transferred as one block is small, increase in the quantity of read/write data entails a correspondingly large number of command entries. Accordingly, auto-precharge type DRAM (Dynamic Random Access Memory) which performs read operation and precharge operation at the same time in response to a single entry of command, SRAM (Static RAM) which requires no precharge operation, etc. are useful for the purpose.

[0004] This will be explained with reference to FIGS. 15 and 16.

[0005] FIGS. 15(A), 15(B) and 15(C) illustrate the operation of a DRAM with no auto-precharge function, that is, a non-auto-precharge type DRAM wherein the number of data bits read out at a time is two. In the case of the non-auto-precharge type DRAM, a precharge command (PRE1 - PRE3) needs to be entered following the access in order to execute precharge operation, as shown in FIG. 15(B). In the illustrated example, read commands (RD1 - RD3) are input respectively at the leading edges of the zeroth, second and fourth basic clock pulses (FIG. 15(A)), and precharge commands (PRE1 - PRE3) are input respectively at the leading edges of the first, third and fifth clock pulses. As a result of the entry of the read commands, 2-bit blocks of data (Q11, Q12; Q21, Q22; Q31, Q32) are output from a DATA output terminal at the leading edges of the first, third and fifth clock pulses, respectively, as shown in FIG. 15(C).

[0006] FIGS. 16(A), 16(B) and 16(C) illustrate the operation of an auto-precharge type DRAM capable of automatic precharge operation wherein the number of data bits read out at a time is two. As shown in the figures, in the case of the auto-precharge type DRAM, no precharge command needs to be entered, so that the read commands (RD1 - RD3) can be continuously input, as seen from FIG. 16(B). Also, since the interval between commands can be shortened, the interval between data (Q11, Q12, Q21, Q22, Q31, Q32) output from the DATA output terminal is shorter than in the case of FIG. 15, as seen from FIG. 16(C). Compared with the case shown in FIG. 15, therefore, all data can be read out in a shorter period of time.

[0007] As explained above, where the number of data bits exchanged between the semiconductor memory

device and the control device therefor is small, a device capable of automatic precharge operation, like the auto-precharge type DRAM, is useful because it ensures relatively high density of commands and as a consequence, higher data access density.

[0008] The foregoing explains the case where the number of data bits exchanged between the semiconductor memory device and the control device therefor is small; in the following will be considered a case where the number of bits is large.

[0009] FIGS. 17(A), 17(B) and 17(C) illustrate the operation of an auto-precharge type DRAM wherein the number of data bits exchanged with the control device is eight. In the illustrated example, a read command RD1 (FIG. 17(B)) is input at the leading edge of the zeroth basic clock pulse shown in FIG. 17(A), and as a result, readout data is output from the DATA output terminal, as shown in FIG. 17(C).

[0010] FIGS. 18(A), 18(B) and 18(C) illustrate the operation of an auto-precharge type DRAM wherein the number of data bits exchanged with the control device is eight and the number of data bits read out at a time is two.

[0011] As shown in the figures, in the case where a DRAM from which two bits of data can be read out at a time is applied to a system in which the number of data bits exchanged with the control device is eight, four RD commands (RD1 - RD4) need to be input. Since, as a result, the interval between the RD commands becomes shorter, an inconvenience arises in that during the access other devices are unable to access the DRAM.

[0012] There have also been proposed semiconductor memory devices in Unexamined Japanese Patent Publications (KOKAI) Nos. 2-94194 and 7-192458, wherein at the time of write operation, identical data is written into a plurality of memory banks and at the time of read operation, data is sequentially read out from different memory banks, to thereby shorten the random access time during the read operation.

[0013] FIG. 19 illustrates the operation of a clock synchronization type, among semiconductor memory devices of this type. The semiconductor memory device has four memory banks BANK0 to BANK3 for holding identical data. FIG. 19 exemplifies a case where a write cycle intervenes between read cycles.

[0014] Read commands RD1 to RD6 are sequentially supplied in synchronism with a clock signal CLK ((a) in FIG. 19). In response to the read commands RD1 to RD6, the four memory banks BANK0 to BANK3 operate in turn ((b) in FIG. 19), so that readout data Q1 to Q6 are output in succession ((c) in FIG. 19). In the illustrated example, the read operation period of each of the memory banks BANK0 to BANK3 is four clock cycles, but since the memory banks BANK0 to BANK3 operate in parallel, the read cycle corresponds to one clock cycle.

[0015] Following the read command RD6, a write command WR7 is supplied ((d) in FIG. 19). In response to the write command WR7, all of the memory banks

BANK0 to BANK3 perform write operation at the same time. Accordingly, the write command WR7 is supplied after all of the memory banks BANK0 to BANK3 have become idle. In the illustrated example, the write command WR7 needs to be supplied after completion of the operation of the memory bank BANK1. Consequently, a READ-WRITE interval (timing specification) from the supply of the read command RD6 to the supply of the write command WR7 is four clock cycles equal to the operation period of the memory bank BANK1.

[0016] In response to the write command WR7, the four memory banks BANK0 to BANK3 perform the write operation at the same time, and as a result, identical write data D7 is written into the memory banks BANK0 to BANK3 ((e) in FIG. 19). Since the identical write data D7 is written in the four memory banks BANK0 to BANK3 at the same time, the write cycle is equal to four clock cycles corresponding to the write operation period of the memory banks BANK0 to BANK3.

[0017] Subsequently, read commands RD8 to RD11 are sequentially supplied ((f) in FIG. 19). The four memory banks BANK0 to BANK3 operate in turn ((g) in FIG. 19) and readout data Q8 to Q11 are output in succession ((h) in FIG. 19) in the same manner as described above.

[0018] Conventionally, an optimum device must be selected in accordance with the number of data bits exchanged between the semiconductor memory device and the control device therefor, as seen from FIGS. 15 to 18. In other words, there was no conventional device that can cope with all probable numbers of bits.

[0019] Also, as shown in FIG. 19, all of the memory banks BANK0 to BANK3 perform write operation at the same time. Accordingly, in cases where a write cycle intervenes between read cycles, the write command WR7 needs to be supplied after the read operations of all memory banks BANK0 to BANK3 are completed. As a result, the supply of the write command WR7 must be deferred for four clock cycles after the supply of the read command RD6. Further, the interval (READ-READ command interval) required from the read command RD6 to the next read command RD8 corresponds to the sum of the operation period of the memory bank BANK1 which is the last to perform the read operation and the write operation period.

[0020] As a consequence, especially in cases where read cycles and write cycles take place randomly, a problem arises in that the data transfer rate (data bus occupancy) lowers.

[0021] The present invention was created in view of the above circumstances, and an embodiment may provide a semiconductor memory device which enables optimum operation regardless of the number of data bits exchanged with a control device for controlling the semiconductor memory device, and an information processing system including such a semiconductor memory device.

[0022] An embodiment of the present invention can shorten the operation cycle time of the semiconductor

memory device, in particular, to shorten a command supply interval during random access, thereby enhancing the transfer rate of input/output data.

[0023] An aspect of the invention provides an information processing system including a semiconductor memory device having  $n$  ( $n > 1$ ) banks and a control device for controlling the semiconductor memory device. The semiconductor memory device comprises an address input circuit for receiving an input address, a readout circuit for sequentially reading, from  $m$  ( $\leq n$ ) banks, data corresponding to one address input via the address input circuit, and a data output circuit for outputting the data read by the readout circuit from the  $m$  banks to outside as collective data. The control device comprises a control circuit for controlling the semiconductor memory device in accordance with a cycle time determined by a read cycle of the readout circuit, and an access inhibit circuit for inhibiting access to a predetermined bank in accordance with the bank from which data is being read by the readout circuit.

[0024] Reference is made, by way of example only, to the accompanying drawings in which:

FIG. 1 is a diagram illustrating the principle of operation according to the present invention;  
 FIGS. 2(A), 2(B) and 2(C) are a timing chart outlining the operation in accordance with the principle illustrated in FIG. 1;  
 FIG. 3 is a diagram showing an exemplary configuration according to an embodiment of the present invention;  
 FIG. 4 is a diagram showing in detail an exemplary configuration of a semiconductor memory device appearing in FIG. 3;  
 FIG. 5 is a diagram showing in detail an exemplary configuration of a control section appearing in FIG. 4;  
 FIG. 6 is a diagram showing in detail exemplary configurations of a bank activation control circuit, a timing circuit and an ADD latch, all appearing in FIG. 5;  
 FIG. 7 is a circuit diagram showing in detail an exemplary configuration of a DFF element appearing in FIG. 6;  
 FIG. 8 is a timing chart illustrating an operation according to the embodiment shown in FIG. 2;  
 FIG. 9 is a timing chart also illustrating the operation according to the embodiment shown in FIG. 2;  
 FIG. 10 is a block diagram showing a second embodiment;  
 FIG. 11 is a block diagram showing details of a bank selection circuit appearing in FIG. 10;  
 FIG. 12 is a timing chart illustrating an operation according to the second embodiment;  
 FIG. 13 is a block diagram showing a third embodiment;  
 FIG. 14 is a timing chart illustrating an operation according to the third embodiment;

FIGS. 15(A), 15(B) and 15(C) are a timing chart illustrating an operation of a conventional semiconductor memory device;

FIGS. 16(A), 16(B) and 16(C) are a timing chart illustrating an operation of another conventional semiconductor memory device;

FIGS. 17(A), 17(B) and 17(C) are a timing chart illustrating an operation of still another conventional semiconductor memory device;

FIGS. 18(A), 18(B) and 18(C) are a timing chart illustrating an operation of yet another conventional semiconductor memory device; and

FIG. 19 is a timing chart illustrating an operation of a conventional semiconductor memory device.

[0025] Embodiments of the present invention will be hereinafter described with reference to the drawings. FIG. 1 illustrates the principle of operation according to the present invention. As shown in the figure, a semiconductor memory device according to the present invention comprises an address input circuit 1, a readout circuit 2, a data output circuit 3, an output data quantity setting circuit 4, and banks 5-1 to 5-n.

[0026] The address input circuit 1 receives an address input thereto for access from outside.

[0027] The readout circuit 2 sequentially reads, from  $m ( \leq n )$  banks, data corresponding to one address input via the address input circuit 1.

[0028] The data output circuit 3 outputs the data read by the readout circuit 2 from the  $m$  banks to outside as collective data.

[0029] The output data quantity setting circuit 4 sets the quantity of data to be output from the data output circuit 3.

[0030] Operation in accordance with the illustrated principle will be now described.

[0031] At the start of operation of the semiconductor memory device, for example, the output data quantity setting circuit 4 receives, as a control signal from a control device, not shown, information for specifying a quantity of data to be output from the data output circuit 3 as collective data, and sets the output data quantity in accordance with the received information.

[0032] With the data quantity to be output from the data output circuit 3 as collective data set in this manner, an address is input to the address input circuit 1 from outside, whereupon the address input circuit 1 supplies the input address to the readout circuit 2.

[0033] If the data quantity set by the output data quantity setting circuit 4 is larger than a quantity of data that can be read at a time from a single bank, the readout circuit 2 first selects a bank corresponding to the address input from the address input circuit 1, then reads data from the selected bank and outputs the data to the data output circuit 3. Subsequently, the readout circuit 2 performs bank switching and acquires other data from the same address of a different bank newly switched to. Operation like this is repeated until the quantity of re-

dout data reaches the output data quantity specified by the output data quantity setting circuit 4. In this case, the readout circuit 2 reads data from the banks at predetermined intervals of time so that the data read from different banks may not be congested.

[0034] The data output circuit 3 sequentially acquires the data read by the readout circuit 2 from the banks 5-1 to 5-n, and outputs the data successively to outside.

[0035] Thus, if the data quantity to be output from the data output circuit 3 as collective data is equal to or smaller than the quantity of data that can be read at a time from a single bank, the readout circuit 2 reads data from one bank and then terminates the read operation; on the other hand, if the former is larger than the latter, the readout circuit 2 sequentially reads, from different banks, data corresponding to one address supplied from the address input circuit 1 while automatically switching the banks 5-1 to 5-n.

[0036] Consequently, the quantity of data read out by a single addressing can be varied in accordance with the quantity of data (collective data) which is exchanged with the control device and which is determined by an application in use, making it possible to provide a semiconductor memory device which serves a diversity of uses.

[0037] FIGS. 2(A), 2(B) and 2(C) illustrate an example of operation in the case where the number of banks is four ( $n = 4$ ), the number of data bits read from a single bank at a time is two, and the number of data bits output from the data output circuit 3 as collective data is set to eight.

[0038] In the illustrated example, a read command RD1 is input in synchronism with the leading edge of the zeroth basic clock pulse shown in FIG. 2(A). In this case, since the number of data bits read from a single bank at a time is two, the readout circuit 2 switches the four banks in turn, sequentially reads, from the individual banks, data corresponding to one address input from the address input circuit 1, and supplies the readout data to the data output circuit 3. The data output circuit 3 outputs the data (Q11, Q12, ..., Q41, Q42), which the circuit 3 has received separately over four times from the readout circuit 2, to outside as collective data, as shown in FIG. 2(C).

[0039] Thus, compared with the conventional semiconductor memory device in which the read command needs to be input four times as indicated by the broken lines in FIG. 2(B), a single entry of read command suffices.

[0040] In the above example, the readout circuit 2 makes reference to the data output circuit 3 to detect the data quantity set by the output data quantity setting circuit 4, but the readout circuit may alternatively detect the set data quantity by directly referring to the output data quantity setting circuit 4.

[0041] An embodiment of the present invention will be now described.

[0042] FIG. 3 shows an exemplary configuration of an

information processing system according to the embodiment of the present invention, which embodiment corresponds to claims 1 to 4. As shown in the figure, the information processing system of the present invention comprises a CPU (Central Processing Unit) 10, a control device 20, a semiconductor memory device 30, and a bus 40.

[0043] The CPU 10 executes various programs etc. stored in the semiconductor memory device 30, to control the individual parts of the system and to perform various operations.

[0044] The control device 20 performs control operations relating to the burst length setting, refreshing, etc. of the semiconductor memory device 30.

[0045] The semiconductor memory device 30 operates under the control of the control device 20 to store data supplied from the CPU 10 and to supply the stored data read-out therefrom to the CPU 10.

[0046] The bus 40 transmits data from the CPU 10 to the semiconductor memory device 30 and vice versa.

[0047] FIG. 4 shows in detail an exemplary configuration of the semiconductor memory device 30 appearing in FIG. 3. As shown in the figure, the semiconductor memory device 30 comprises a control section 50, a bank A 60, and a bank B 70. The bank A 60 is constituted by a cell 61, a column decoder 62, a row decoder 63, an SA (Sense Amplifier) 64, and an I/O (Input/Output) circuit 65. Similarly, the bank B 70 is constituted by a cell 71, a column decoder 72, a row decoder 73, an SA 74, and an I/O circuit 75.

[0048] The control section 50 is input with a CLK signal, CMD signal, ADD signal, DATA signal, etc. and supplies the signals to the respective parts of the device. Also, when transferring data, the control section selects a predetermined bank to read or write data from or into the selected bank.

[0049] The cell 61 of the bank A 60 comprises a group of memory elements arranged in matrix form and stores input data.

[0050] The row decoder 63 specifies a certain row of the cell 61 in accordance with a row address when inputting/outputting data.

[0051] The column decoder 62 specifies a certain column of the cell 61 in accordance with a column address when inputting/outputting data.

[0052] The SA 64 amplifies a signal read from the cell 61 with a predetermined gain, to convert the signal level to a digital signal level.

[0053] The I/O circuit 65 performs control operation relating to the input/output of data.

[0054] The bank B 70 is configured in the same manner, and therefore, description thereof is omitted.

[0055] FIG. 5 shows in detail an exemplary configuration of the control section 50 appearing in FIG. 4.

[0056] A CLK input terminal 80 is input with the CLK signal from outside. A CMD input terminal 81 is input with the CMD signal from outside, and an ADD input terminal 82 is input with the ADD signal from outside.

[0057] A CLK input circuit 83 shapes the waveform of the CLK signal input from the CLK input terminal 80, and then supplies the shaped CLK signal to a CMD input circuit 84, an ADD input circuit 85 and a bank activation control circuit 88.

[0058] The CMD input circuit 84 shapes the waveform of the CMD signal input from the CMD input terminal 81, and then supplies the shaped CMD signal to a CMD decoder 86.

[0059] The ADD input circuit 85 shapes the waveform of the ADD signal input from the ADD input terminal 82, and then supplies the shaped ADD signal to a burst length determination circuit 87.

[0060] The CMD decoder 86 decodes the CMD signal supplied from the CMD input circuit 84, and supplies the obtained RD or WR command to the bank activation control circuit 88 and an ADD latch 90.

[0061] At the start of operation of the device, for example, the burst length determination circuit 87 is supplied with a command to set the burst length, whereupon the circuit 87 analyzes the command to determine the burst length requested to be set, and notifies the bank activation control circuit 88 of the determined burst length.

[0062] The bank activation control circuit 88, a timing circuit 89 and the ADD latch 90, which are provided for each of the banks A 60 and B 70 shown in FIG. 4, supply an internal address IADD to the bank associated therewith and control the data read operation.

[0063] The bank activation control circuit 88 controls the timing circuit 89 in accordance with the set burst length, to control the operation of reading data from the corresponding bank.

[0064] The ADD latch 90 latches the ADD signal output from the ADD input circuit 85, in synchronism with the RD command output from the CMD decoder 86.

[0065] The timing circuit 89 supplies the ADD signal latched by the ADD latch 90, to the corresponding bank as the internal address IADD at the timing as controlled by the bank activation control circuit 88.

[0066] FIG. 6 shows in detail exemplary configurations of the bank activation control circuit 88, the timing circuit 89 and the ADD latch 90.

[0067] As shown in the figure, the bank activation control circuit 88 comprises inverters 100 to 102, NOR elements 103 and 104, a NAND element 105, DFF (Data Flip-Flop) elements 106 to 109, and CMOS (Complementary Metal-Oxide Semiconductor) switches 110 and 111.

[0068] The inverter 100 inverts the RD/WR signal input from the CMD decoder 86, and supplies the inverted signal to the NOR element 103. The NOR element 104 supplies the NOR element 103 with the result of inversion of a logical sum of the ADD signal input from the ADD input circuit 85 for specifying a bank and a BL8 signal (signal which turns to the "H" state when the burst length is set to "8") supplied from the burst length determination circuit 87.

[0069] The NAND element 105 supplies the NOR element 103 with the RD/WR signal input from the CMD decoder 86 and the ADD signal input from the ADD input circuit 85. The NOR element 103 supplies the DFF element 106 with the result of inversion of the logical sum of the RD/WR signal input from the CMD decoder 86 and the ADD signal input from the ADD input circuit 85.

[0069] The NOR element 103 supplies the DFF element 106 with the result of inversion of a logical sum of the outputs from the inverter 100 and the NOR element 104.

[0070] The DFF elements 106 to 108 sequentially delay the output of the NOR element 103 in synchronism with the trailing edge of the CLK signal. The output of the DFF element 108 is supplied to the CMOS switch 110.

[0071] The DFF element 109 latches the output of the NOR element 103 in synchronism with the trailing edge of the CLK signal, and supplies the latched signal to the CMOS switch 111.

[0072] The inverter 101 inverts the ADD signal and outputs the inverted signal to the NAND element 105, which then supplies the inverter 102 and the CMOS switches 110 and 111 with the result of inversion of a logical product of the output from the inverter 101 and the BL8 signal.

[0073] The CMOS switch 110 turns ON when the output of the NAND element 105 is in the "L" state, to supply the output of the DFF element 108 to the timing circuit 89 as a BACT signal, and turns OFF when the output of the NAND element 105 is in the "H" state.

[0074] The CMOS switch 111 turns ON when the output of the NAND element 105 is in the "H" state, to supply the output of the DFF element 109 to the timing circuit 89 as the BACT signal, and turns OFF when the output of the NAND element 105 is in the "L" state.

[0075] Accordingly, when the output of the NAND element 105 turns to "H", the CMOS switch 111 turns ON and the output of the DFF element 109 is supplied to the timing circuit 89 as the BACT signal; when the output of the NAND element 105 turns to "L", the CMOS switch 110 turns ON and the output of the DFF element 108 is supplied to the timing circuit 89 as the BACT signal.

[0076] The ADD latch 90 is constituted by an inverter 130 and a DFF element 131. The inverter 130 inverts the RD/WR signal and outputs the inverted signal to the DFF element 131, which then latches the ADD signal in synchronism with the trailing edge of the output from the inverter 130, that is, the leading edge of the RD/WR signal, and outputs the latched signal as a BADD signal.

[0077] The timing circuit 89 comprises an inverter 120 and a DFF element 121. The inverter 120 inverts the BACT signal which is the output of the CMOS switch 110. The DFF element 121 latches the BADD signal in synchronism with the trailing edge of the output from the inverter 120, that is, the leading edge of the BACT signal, and outputs the latched signal as the internal address IADD signal to the bank A 60 or the bank B 70.

[0078] FIG. 7 shows in detail an exemplary configuration of the DFF elements 106 to 109 appearing in FIG. 6. As shown in the figure, each DFF element comprises inverters 140 to 144, and CMOS switches 145 and 146.

[0079] The inverter 140 inverts the CLK signal and supplies the inverted signal to the CMOS switches 145 and 146.

[0080] When the clock signal turns to "H", the CMOS switch 145 turns ON and supplies the input signal to the inverter 141.

[0081] When the clock signal turns to "L", the CMOS switch 146 turns ON and supplies the output of the inverter 141 to the inverter 143.

[0082] The inverter 141 inverts the output of the CMOS switch 145 and supplies the inverted output to the CMOS switch 146.

[0083] The inverter 142 inverts the output of the inverter 141 and feeds the inverted output back to the input of the inverter 141.

[0084] The inverter 143 inverts the output of the CMOS switch 146 and outputs the resulting signal.

[0085] The inverter 144 inverts the output of the inverter 143 and feeds the inverted output back to the input of the inverter 143.

[0086] Operation of the above embodiment will be now described.

[0087] When the power supply to the information processing system shown in FIG. 3 is started, the CPU 10 notifies the control device 20 of the number of data bits to be exchanged with the semiconductor memory device 30 in accordance with an application to be executed.

[0088] In accordance with the number of data bits notified from the CPU 10, the control device 20 sets a burst length for the semiconductor memory device 30. For example, in the case where the data bit length that can be

read at a time from the bank A 60 or B 70 of the semiconductor memory device 30 is four and "8 bits" is set as the burst length, the control device 20 inputs a command for setting the burst length to the CMD input terminal 81 of the semiconductor memory device 30, as

well as data indicative of the burst length "8" to the ADD input terminal 82. Although conventional semiconductor memory devices do not permit the burst length to be set to a length exceeding the number of data bits that can be read at a time from a bank thereof, such burst length setting can be performed in this embodiment.

[0089] As a result, the CMD decoder 86 detects the input of the command for setting the burst length, and requests the burst length determination circuit 87 to set the burst length. The burst length determination circuit

87 decodes the data supplied from the ADD input circuit 85 and recognizes that the burst length should be set to "8". Then, the circuit 87 turns the BL8 signal (signal which is set in the "H" state when the burst length is "8") to the "H" state, the BL8 signal being supplied to the bank activation control circuits 88 associated with the respective banks A 60 and B 70.

[0090] While in this state, if a read command to read data from the bank A 60 is input, the bank activation control circuit 88 of the bank A 60 operates in the manner described below with reference to FIGS. 8 and 9.

[0091] Let it be assumed that an RD command is input in synchronism with the leading edge of the zeroth clock pulse, as shown in (B) of FIG. 8, and that an address

((C) in FIG. 8) selecting the bank A 60 is supplied from the ADD input circuit 85.

[0092] The DFF elements 106 to 108 sequentially delay the output signal of the NOR element 103 in synchronism with the trailing edge of the CLK signal, and provide output signals N1 to N3, respectively ((H)-(J) in FIG. 8).

[0093] The DFF element 109 latches the output signal of the NOR element 103 in synchronism with the trailing edge of the CLK signal, and provides an output signal N4 ((K) in FIG. 8).

[0094] At this time, the output of the NAND element 105 in the bank activation control circuit 88 of the bank A 60 is in the "H" state, as shown in (F) of FIG. 8, and an N5 signal, which is the output of the inverter 102, is in the "L" state, as shown in (E) of FIG. 8, so that the CMOS switch 111 is in the ON state. Consequently, the N4 signal ((K) in FIG. 8), which is the output of the DFF element 109, is selected and supplied to the timing circuit 89 as the BACT signal ((L) in FIG. 8).

[0095] The ADD latch 90 latches the ADD signal in synchronism with the leading edge of the RD/WR signal, and supplies the latched signal to the timing circuit 89 as the BADD signal ((M) in FIG. 8).

[0096] The timing circuit 89 latches the BADD signal in synchronism with the leading edge of the BACT signal, and supplies the latched signal to the bank A 60 as the IADD signal ((N) in FIG. 8).

[0097] As a result, the bank A 60 reads data from the specified address and outputs the readout data from a DATA output terminal ((O) in FIG. 8), not shown.

[0098] At this time, in the bank activation control circuit 88 of the bank B 70, the N5 signal ((E) in FIG. 9) is in the "H" state while the N6 signal ((F) in FIG. 9) is in the "L" state, so that the output of the DFF element 108 is selected and supplied to the timing circuit 89.

[0099] The N3 signal ((J) in FIG. 9), which is the output of the DFF element 108, is derived by delaying the N1 signal ((H) in FIG. 9) for two cycles of the CLK signal, and accordingly, the BADD signal ((M) in FIG. 9) latched by the ADD latch 90 is supplied to the bank B 70 as the IADD signal while being delayed for two cycles of the CLK signal with respect to the IADD signal supplied to the bank A 60.

[0100] The bank B 70 reads out data stored at the address specified by the IADD signal supplied from the timing circuit 89, and outputs the readout data to outside from a DATA output terminal, not shown.

[0101] As a consequence, where the burst length has been set to "8", data is first read from one specified bank (in the above example, the bank A 60), and then data is read from the other bank (in the above example, the bank B 70) in an automatic manner (without the need for the reentry of address from outside) with a delay of two cycles of the CLK signal and is output to outside.

[0102] In the case where the semiconductor memory device 30 is an auto-precharge type device, auto-precharge operation is carried out upon completion of the

read operation of the other bank.

[0103] In the aforementioned example, the bank A 60 is specified first and then the bank B 70 is specified. Also in the case where the bank B 70 is specified first and the bank A 60 is specified next, similar operation is executed and 8-bit data is output.

[0104] The foregoing describes the operation wherein the burst length is set to "8"; in cases where the burst length is set to "4" or a smaller value, data is read from only one of the banks and is output, as in the conventional memory devices.

[0105] Specifically, where the burst length is set to a value other than "8", the BL8 signal is set in the "L" state. Accordingly, the outputs of the NAND elements 105 of the respective banks A 60 and B 70 are always in the "H" state, and as a consequence, the CMOS switches 111 remain in the ON state.

[0106] In this case, the output of the NOR element 104 turns to "L" when the bank managed thereby is specified, and turns to "H" during the other period of time. Consequently, the NOR element 103 passes the RD/WR signal therethrough only while the bank associated therewith is selected, and shuts off the signal while the other bank is specified.

[0107] As a result, while the bank is specified, the signal output from the corresponding DFF element 109 is supplied to the timing circuit 89 as the BACT signal, and the BADD signal latched by the ADD latch 90 is supplied to the bank as the IADD signal in synchronism with the leading edge of the BACT signal.

[0108] Accordingly, where the burst length is set to "4", for example, IADD is supplied only to the bank specified by the bank-specifying address, and data stored in the corresponding address is read and is output to outside from the DATA output terminal, not shown, whereupon the operation is completed.

[0109] In the case where the burst length is set to "8", while one of the banks is accessed, the other bank cannot be accessed. If an interrupt request is made with respect to a bank other than the bank being accessed, therefore, the control device 20 performs a process for inhibiting execution of such an interrupt request.

[0110] Also, where the burst length is set to "8", a total of the time periods required to read data from the two banks constitutes a cycle time. Accordingly, the control device 20 determines the cycle time in accordance with the burst length, and performs control operation suited for the determined cycle time.

[0111] In the above description of the embodiment, the banks used are two in number, but the present invention can of course be applied to memory configurations including three or more banks.

[0112] Also, it is to be noted that the circuitry explained and illustrated in conjunction with the above embodiment is given by way of example only, and that the present invention is of course not limited to the illustrated circuitry.

[0113] FIG. 10 shows a semiconductor memory de-

vice according to a second embodiment of the present invention, the second embodiment corresponding to claims 6 to 8. In the figure, each thick line signifies that the line comprises a plurality of signal lines.

[0114] The semiconductor memory device is formed using a CMOS process on a silicon substrate as a clock synchronization type DRAM. The DRAM comprises a clock buffer 210, a command decoder 212, an address buffer 214, a data buffer 216, a write timing generator circuit 218, a bank selection circuit 220, a write data register 222, and four memory banks BANK0 to BANK3.

[0115] The clock buffer 210 receives a clock signal CLK from outside through a clock terminal, and outputs the received signal as an internal clock signal ICLK. The internal clock signal ICLK is supplied also to other circuits than those illustrated.

[0116] The command decoder 212 receives a command signal CMD from outside through a command terminal, decodes the received signal, and outputs the decoded signal as a read command signal READ1 and a write command signal WRITE1. The command decoder 212 outputs a refresh command signal etc., besides the illustrated signals.

[0117] The address buffer 214 receives an address signal ADD from outside through an address terminal, and outputs the received signal as an internal address signal IADD. The data buffer 216 receives a data signal (write data) DQ from outside through a data terminal, and outputs the received signal to the write data register 222. Also, the data buffer 216 receives an internal data signal (readout data) IDQ from the memory banks BANK0 to BANK3, and outputs the received signal via the data terminal as the data signal DQ. The write data register 222 latches the write data and outputs the latched data as the internal data signal IDQ (latched data signal LDATA).

[0118] The write timing generator circuit 218 receives the write command signal WRITE1 and the internal clock signal ICLK, and outputs a write command signal (write timing signal) WRITE2 in synchronism with the internal clock signal ICLK. The write command signal WRITE2 is generated four times consecutively in response to one write command signal WRITE1, as described later.

[0119] The bank selection circuit 220 activates one of bank selection signals BKSEL0 to BKSEL3 synchronously with activation of the read command signal READ1 and the write command signal WRITE2.

[0120] The memory banks BANK0 to BANK3 have identical addresses assigned thereto and each have a storage capacity of 16 Megabits, for example. Thus, the write data DQ supplied in response to the write command is written into all of the memory banks BANK0 to BANK3, as described later. Namely, this DRAM is used as a 16-Megabit memory, though it has a total storage capacity of 64 Megabits.

[0121] Also, although not illustrated in detail, the memory banks BANK0 to BANK3 each have a plurality

of memory cells connected to word lines and bit lines; sense amplifiers for amplifying data transmitted onto the bit lines, column switches connecting the bit lines and a data bus line, a row decoder, and a column decoder.

5 The row decoder activates a sense amplifier and selects a word line in accordance with a high-order address signal ADD. The column decoder selects a column switch in accordance with a low-order address signal ADD.

[0122] In this embodiment, the high-order and low-order address signals ADD are input to the DRAM collectively along with the read command and the write command. Namely, the DRAM is an address non-multiplex type semiconductor memory. The memory banks BANK0 to BANK3 operate independently of one another and, after the operation, automatically precharge the bit lines under their own control.

[0123] FIG. 11 shows details of the bank selection circuit 220 appearing in FIG. 10. The bank selection circuit 220 includes an OR element 220a and a shift register 220b. The OR element 220a derives an OR of the read command signal READ1 and the write command signal WRITE2, and outputs the result as a shift signal SFT. The shift register 220b has four storage stages S0 to S3 connected in series.

25 [0124] The storage stages S0 to S3 output the bank selection signals BKSEL0 to BKSEL3, respectively. The output (BKSEL3) of the storage stage S3 is fed back to the input of the storage stage S0. Each of the storage stages S0 to S3 operates in synchronism with the shift signal SFT, to output the value retained thereby to the succeeding stage.

[0125] The shift register 220b is initialized after the start of power supply such that only the bank selection signal BKSEL0 has a high-level output. Subsequently, each time the read command signal READ1 or the write command signal WRITE2 is activated, the shift register 220b performs a shift operation to sequentially turn the bank selection signals BKSEL1, BKSEL2, BKSEL3, BKSEL0, ... to high level. When one of the bank selection signals BKSEL0 to BKSEL3 is activated, a corresponding one of the memory banks BANK0 to BANK3 is set operable.

[0126] FIG. 12 illustrates operation of the DRAM described above. In the example shown in FIG. 12, first, 45 read commands RD1 to RD6 are sequentially supplied, and then a write command WR7 is supplied, followed by the supply of read commands RD8 to RD11. Each command is supplied in synchronism with the leading edge of the clock signal CLK.

50 [0127] First, the command decoder 212 shown in FIG. 10 receives the read command RD1 and activates the read command signal READ1 ((a) in FIG. 12). In synchronism with the read command signal READ1, the bank selection circuit 220 activates the bank selection signal BKSEL0 ((b) in FIG. 12). The memory bank BANK0 is thereafter activated in response to the bank selection signal BKSEL0 ((c) in FIG. 12).

[0128] In accordance with the high-order address sig-

nal ADD (not shown), the memory bank BANK0 selects a word line and activates a sense amplifier. The selection of a word line permits data to be read from a corresponding memory cell to the bit line, and the readout data is amplified by the sense amplifier. Further, in accordance with the low-order address signal ADD, the memory bank BANK0 selects a column switch to transmit the readout data, amplified by the sense amplifier, to the data bus line.

[0129] The readout data Q1 read from the memory cell is output in synchronism with the leading edge of a clock signal CLK pulse two cycles later than the supply of the read command RD1 ((d) in FIG. 12). Namely, a read latency, which is expressed as the number of clock pulses from the supply of the read command RD1 to the output of the readout data Q1, is "2".

[0130] Subsequently, the memory bank BANK0 inactivates the sense amplifier and the row and column decoders, executes a precharge operation in which the bit line is set to a reference voltage, and completes the read operation four clock cycles after the reception of the read command RD1 ((e) in FIG. 12).

[0131] Then, in response to the read command RD2, the read command signal READ1 is activated again ((f) in FIG. 12). The shift register 220b of the bank selection circuit 220 performs a shift operation synchronously with the read command signal READ1, thereby inactivating the bank selection signal BKSEL0 and activating the bank selection signal BKSEL1 ((g) in FIG. 12). Subsequently, in response to the bank selection signal BKSEL1, the memory bank BANK1 is activated. The memory bank BANK1 performs a read operation in the same manner as performed by the memory bank BANK0, and outputs readout data Q2 ((h) in FIG. 12).

[0132] Subsequently, in response to the read commands RD3 to RD6, the bank selection signals BKSEL2, BKSEL3, BKSEL0 and BKSEL1 are sequentially activated ((i) in FIG. 12), and the memory banks BANK2, BANK3, BANK0 and BANK1 successively carry out read operation in the same manner as described above ((j) in FIG. 12).

[0133] Thus, the read operations of the four memory banks BANK0 to BANK3 are carried out in a manner such that one read operation overlaps with another while being staggered therefrom by one clock cycle. The operation period of one memory bank BANK is four clock cycles, but since the four memory banks BANK0 to BANK3 operate independently of each other, the read cycle, which is a read operation time (read command RD supply interval) required for one read command RD, corresponds to one clock cycle.

[0134] The write command WR7 is supplied two clock cycles after the supply of the read command RD6 ((k) in FIG. 12). As distinct from the conventional device, some of the memory banks BANK (in this example, BANK0 and BANK1) are executing read operations when the write command WR7 is supplied. In this manner, write operation for writing data in an idle memory

bank BANK is started while some of the memory banks BANK are still in operation, whereby the READ-WRITE interval (timing specification) from the supply of the read command RD6 to the supply of the write command WR7

5 can be set to two clock cycles. This interval is shorter by two clock cycles than in the case of the conventional device shown in FIG. 19. More specifically, the READ-WRITE interval is set to a timing such that contention between the data bus line and the data terminal

10 can be avoided when a write latency is "2" (mentioned later).

[0135] The command decoder 212 receives the write command WR7 and activates the write command signal WRITE1 for four clock cycles ((l) in FIG. 12). During

15 the period in which the write command signal WRITE1 remains activated, the write timing generator circuit 218 generates the write command signal (write timing signal) WRITE2 in synchronism with the clock signal CLK (internal clock signal ICLK) ((m) in FIG. 12). Specifically,

20 the write command signal WRITE2 is activated four times consecutively, corresponding to the number of the memory banks BANK0 to BANK3. In synchronism with the write command signal WRITE2, the bank selection circuit 220 sequentially activates the bank selection signals BKSEL2, BKSEL3, BKSEL0 and BKSEL1 ((n) in FIG. 12). In response to the bank selection signals BKSEL2, BKSEL3, BKSEL0 and BKSEL1, the memory banks BANK2, BANK3, BANK0 and BANK1 are sequentially activated ((o) in FIG. 12).

25 [0136] The OR element 220a of the bank selection circuit 220 outputs the shift signal SFT synchronously with the read command signal READ1 and the write command signal WRITE2. The shift register 220b performs a shift operation in synchronism with the shift signal SFT,

30 thereby sequentially activating the bank selection signals BKSEL0 to BKSEL3. In other words, the shift register 220b performs shift operation regardless of whether the input command is the read or write command, to sequentially activate the bank selection signals BKSEL0

35 to BKSEL3, whereby a memory bank for performing read or write operation is sequentially switched among the memory banks BANK0 to BANK3. Thus, the bank selection circuit 220 is constructed simply by using the OR element 220a and the shift register 220b, and this makes it possible to greatly shorten the READ-WRITE interval, compared with the conventional device.

[0137] Write data D7 is supplied two clock cycles after the supply of the write command WR7 ((p) in FIG. 12). Namely, the write latency, which is the number of clock

50 cycles from the supply of the write command WR7 to the supply of the write data D7, is "2". The write data register 222 fetches the write data D7 through the data buffer 216 and holds the fetched data as the latched data signal LDATA ((q) in FIG. 12).

55 [0138] The memory banks BANK2, BANK3, BANK0 and BANK1 then operate sequentially, so that the latched data signal LDATA held by the write data register 222 is written into the memory cells. That is, identical

write data D7 is written into all memory banks BANK0 to BANK3.

[0139] The memory bank BANK2, which is the first to perform the write operation, becomes idle four clock cycles after the supply of the write command WR7. Accordingly, even though the write operations performed by the memory banks BANK0 to BANK3 are staggered, the read command RD8 can be supplied four clock cycles after the supply of the write command WR7 ((r) in FIG. 12). Namely, the write cycle required for one write command WR is four clock cycles, equal to that in the case of the conventional device.

[0140] In response to the read command RD8, the memory bank BANK2 operates and outputs readout data Q8 ((s) in FIG. 12). Subsequently, the read commands RD9 to RD11 are sequentially supplied, so that the memory banks BANK3, BANK0 and BANK1 sequentially perform read operation and output readout data Q8 to Q11 in the same manner as described above ((t) in FIG. 12).

[0141] As explained above, in this embodiment, the write timing generator circuit 218 consecutively generates, in response to one write command WR, the write command signal (write timing signal) WRITE2 a number of times corresponding to the number of the memory banks BANK0 to BANK3. During write operation, the bank selection circuit 220 sequentially activates the bank selection signals BKSEL0 to BKSEL3 in synchronism with the write timing signal WRITE2. Consequently, the write operations of all memory banks BANK0 to BANK3 can be easily carried out in response to one write command WR with their start timings staggered.

[0142] Also, write operation can be started before all of the memory banks BANK0 to BANK3 become idle, so that the interval from the supply of the read command RD to the supply of the write command WR can be shortened. Further, in cases where read commands RD are supplied with a write command WR intervening therebetween, the read command RD supply interval can be shortened as compared with the conventional device, making it possible to increase the number of commands supplied per given time. Thus, since the data signal can be input/output more frequently than in the conventional device, the data transfer rate (data bus occupancy) improves, and as a result, the performance of the system to which the DRAM is mounted can be enhanced.

[0143] Further, the bank selection circuit 220 comprises the shift register 220b which is simple in construction, and this permits the data transfer rate to be improved without increasing the chip size of the DRAM.

[0144] FIG. 13 shows a semiconductor memory device according to a third embodiment of the present invention, the third embodiment corresponding to claims 6 to 10. Identical reference numerals and symbols are used to denote circuits and signals identical with those explained above in relation to the second embodiment, and detailed description of such circuits and signals is omitted.

[0145] Compared with the second embodiment, the third embodiment is additionally provided with a late write function. The late write function is a function whereby write data supplied in association with a write

5 command is written into the memory cells when the succeeding write command is supplied. The late write function serves to narrow down the timing of contention between readout data and write data, thus improving the efficiency of use of the data bus. In order to perform the late write function, the third embodiment is additionally provided with a delay circuit 224, a write register 226, an address switching circuit 228, an address comparator circuit 230, a data switching circuit 232 and a transfer gate 234, compared with the second embodiment. In 10 other respects, the third embodiment is configured in almost the same manner as the second embodiment. Namely, the semiconductor memory device is fabricated as a clock synchronization type DRAM.

[0146] The delay circuit 224 delays the write command signal WRITE1 for a time period corresponding to the write latency (in this embodiment, "3"), and outputs the delayed signal to the write register 226. The write register 226 includes an address register 226a and a data register 226b which operate in synchronism with 15 the delayed write command signal WRITE1. The address register 226a holds the address signal ADD (internal address signal IADD) and outputs the signal held thereby as a latched address signal LADD. The data register 226b holds the data signal DQ (write data) and 20 outputs the signal held thereby as a latched data signal LDATA.

[0147] The address switching circuit 228 selects the internal address signal IADD when the level of the write command signal WRITE1 is low, and selects the latched 25 address signal LADD when the level of the write command signal WRITE1 is high. Consequently, the memory banks BANK0 to BANK3 operate in accordance with the latched address signal LADD during write operation, and operate in accordance with the external address signal ADD during read operation.

[0148] The address comparator circuit 230 activates (raises the level of) a coincidence signal COIN when the internal address signal IADD coincides with the latched address signal LADD. The address comparator circuit 45 230 determines whether or not the write address is for a memory cell that has not performed the write operation yet.

[0149] The data switching circuit 232 selects the latched data signal LDATA when the level of the coincidence signal COIN is high, and outputs the selected signal as the readout data. When the level of the coincidence signal COIN is low, the data switching circuit selects the internal data signal DQ (readout data) read 50 from the memory banks BANK and outputs the selected signal as the readout data.

[0150] The transfer gate 234 transfers the latched data signal LDATA to the memory banks BANK0 to BANK3 as the internal data signal (write data) DQ when the level

of the write command signal WRITE1 is high. Namely, the write operation is performed using the latched data signal LDATA held by the data register 226b.

[0151] FIG. 14 illustrates operation of the DRAM described above. FIG. 14 shows an example of operation wherein, as in the case of the second embodiment, after read commands RD1 to RD6 are sequentially supplied, a write command WR7 is supplied, followed by the supply of read commands RD8 to RD11. Read operations performed in response to the read commands RD1 to RD6 are identical with those explained above with reference to FIG. 12, and therefore, description thereof is omitted.

[0152] The DRAM of this embodiment has the late write function as mentioned above. The timing for supplying the write command WR7 can therefore be set independently of the timing for supplying the write data D7. This makes it possible to supply the write command WR7 in synchronism with a clock signal CLK pulse immediately after the supply of the read command RD6. Namely, in this embodiment, the READ-WRITE interval (timing specification) from the supply of the read command RD6 to the supply of the write command WR7 can be shortened to one clock cycle. The read cycle and the write cycle are one clock cycle and four clock cycles, respectively, as in the second embodiment.

[0153] In response to the write command WR7, the write command signal WRITE1 is activated for four clock cycles ((a) in FIG. 14). Responsive to the activation of the write command signal WRITE1, the write command signal WRITE2 is activated four times consecutively ((b) in FIG. 14).

[0154] During the period in which the write command signal WRITE1 remains activated, the transfer gate 234 transfers the latched data signal LDATA to the memory banks BANK0 to BANK3. In the illustrated example, write data D0 which has been supplied in association with the preceding write command is sequentially written into all of the memory banks BANK0 to BANK3 synchronously with the write command WR7 ((c) in FIG. 14).

[0155] The write data D7 is supplied three clock cycles after the supply of the write command WR7 ((d) in FIG. 14). Namely, the write latency is set to "3". The write register 226 latches the address signal and the write data D7 in synchronism with the delayed write command signal WRITE1 ((e) in FIG. 14). The write data D7 latched by the write register 226 is written into the memory banks BANK0 to BANK3 in response to the succeeding write command (not shown).

[0156] After a lapse of four clock cycles from the supply of the write command WR7, the read commands RD8 to RD11 are sequentially supplied ((f) in FIG. 14). In response to the read commands RD8 to RD11, the memory banks BANK2, BANK3, BANK0 and BANK1 sequentially perform read operation. It is assumed here that the address signal ADD (not shown) supplied along with the read command RD9 coincides with the latched

address signal LADD held by the address register 226a.

[0157] In this case, the address comparator circuit 230 judges that the address signal ADD supplied along with the read command RD9 coincides with the latched address signal LADD, and accordingly, activates the coincidence signal COIN ((g) in FIG. 14). Namely, it is judged that data to be read out in response to the read command RD9 is not yet written in the memory banks BANK0 to BANK3. Thus, on detecting the activation of

10 the coincidence signal COIN, the data switching circuit 232 outputs, as the readout data, the latched data signal LDATA (write data D7) held by the data register 226b. ((h) in FIG. 14). The read operations in response to the read commands RD8, RD10 and RD11 are performed

15 in the same manner as in the second embodiment.

[0158] This embodiment also provides advantages similar to those achieved by the second embodiment described above. Further, since this embodiment is provided with the write register 226 for holding the write address and write data supplied in association with the write command WR, as well as with the address switching circuit 228 and the transfer gate 234, the write data supplied in association with the write command can be written into the memory cells when the succeeding write

20 command is supplied (late write function). The late write function serves to reduce the combinations of contention between readout data and write data, whereby the efficiency of use of the data bus can be further improved. It is also possible to set the write command WR supply timing independently of the write data supply timing. As a result, the data transfer rate can be further increased.

[0159] The address comparator circuit 230 and the data switching circuit 232 permit correct readout data to be output without fail even in the event that data to be 25 read out in response to the read command RD is not yet written in the memory banks BANK0 to BANK3.

[0160] In the above embodiments, the present invention is applied to clock synchronization type DRAM, by way of example. The application of the present invention 30 is, however, not limited to such DRAM alone, and the invention may be applied to clock synchronization type SRAM, for example. SRAM already has good random accessibility, but by applying the present invention, it is possible to further enhance the data transfer rate.

[0161] In the foregoing description of the embodiments, the present invention is applied, by way of example, to DRAM in which read operation and write operation are performed in response to read and write commands, respectively, but the application of the 35 present invention is not limited to such DRAM alone. For example, the present invention may be applied to DRAM in which a memory bank is activated by an active command and read/write operation is performed in response to a read/write command supplied thereafter.

[0162] While the present invention has been described in detail, it is to be noted that the above embodiments and their modifications are only illustrative of the present invention and that the invention is not limited to

those alone. Obviously the present invention may be modified in various ways without departing from the scope thereof.

[0163] As described above, in the semiconductor memory device according to claim 1, the quantity of data to be read out by a single addressing can be varied, so that the data quantity can be set so as to be best suited to the system. Also, optimizing the data quantity setting for the system makes it possible to shorten the access time.

[0164] In the semiconductor memory device according to claim 2, congestion of data can be prevented. As a consequence, the read interval of time can be set to a permissible minimum value of the semiconductor memory device, whereby the operation speed of the semiconductor memory device can be optimized.

[0165] In the semiconductor memory device according to claim 3, the system allows the output data quantity setting circuit to set a number of bits to be transmitted in the system, so that the number of transmission bits can be set to a desired value by means of software.

[0166] In the semiconductor memory device according to claim 4, after access to a bank is ended, the auto-precharge circuit automatically precharges the bank. This makes it unnecessary to instruct auto-precharge timing from outside, whereby circuitry provided externally to the semiconductor memory device can be simplified.

[0167] With the information processing system according to claim 5, even in cases where an application using a different bit length of data is to be executed, the settings can be changed appropriately in accordance with the required bit length, thus permitting optimum operation.

[0168] The semiconductor memory device according to claim 6 makes it possible to increase the number of commands that can be supplied per given time. Since the data signal can be input/output more frequently than in the conventional device, the data transfer rate (data bus occupancy) improves, and as a result, the performance of the system to which the semiconductor memory device is mounted can be enhanced.

[0169] The semiconductor memory device according to claim 7 uses a shift register which is simple in construction, in order to improve the data transfer rate (data bus occupancy). It is therefore unnecessary to increase the chip size of the semiconductor memory device to enhance the data transfer rate.

[0170] With the semiconductor memory device according to claim 8, all memory banks perform write operation in response to one write command, thus facilitating the write operation.

[0171] The semiconductor memory device according to claim 9 can reduce the combinations of contention between readout data and write data, so that the efficiency of use of the data bus improves. Further, the timing for supplying the write command can be set independently of the timing for supplying the write data, and

as a result, the data transfer rate (data bus occupancy) can be further improved.

[0172] With the semiconductor memory device according to claim 10, even in cases where data to be read out in response to a read command is not yet written into the memory banks because of the late write function, correct readout data can be output without fail.

[0173] The foregoing is considered as illustrative only of the principles of the present invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and applications shown and described, and accordingly, all suitable modifications and equivalents may be regarded as falling within the scope of the invention in the appended claims.

### Claims

- 20 1. A semiconductor memory device having  $n$  ( $n > 1$ ) banks, comprising:
  - an address input circuit for receiving an input address;
  - 25 a readout circuit for sequentially reading, from  $m$  ( $\leq n$ ) banks, data corresponding to one address input via said address input circuit; and a data output circuit for outputting the data read by said readout circuit from the  $m$  banks to outside as collective data.
2. The semiconductor memory device according to claim 1, wherein said readout circuit reads data from the  $m$  banks sequentially at predetermined intervals of time such that congestion of data does not occur.
- 35 3. The semiconductor memory device according to claim 1, further comprising an output data quantity setting circuit for setting a quantity of data to be output from said data output circuit, and
  - 40 wherein said readout circuit sequentially reads data from a number of banks corresponding to the data quantity set by said output data quantity setting circuit.
4. The semiconductor memory device according to claim 1, 2, or 3, further comprising an auto-precharge circuit for automatically precharging each of the banks after access to said each bank is ended.
- 45 5. An information processing system including a semiconductor memory device having  $n$  ( $n > 1$ ) banks, and a control device for controlling the semiconductor memory device, wherein
  - 50 said semiconductor memory device comprises:
    - 55

an address input circuit for receiving an input address;  
 a readout circuit for sequentially reading, from  $m ( \leq n )$  banks, data corresponding to one address input via said address input circuit; and a data output circuit for outputting the data read by said readout circuit from the  $m$  banks to outside as collective data, and  
 said control device comprises:  
 5

a control circuit for controlling said semiconductor memory device in accordance with a cycle time determined by a read cycle of said readout circuit; and  
 an access inhibit circuit for inhibiting access to a predetermined bank in accordance with the bank from which data is being read by said readout circuit.  
 10

6. A semiconductor memory device comprising:  
 20

a plurality of memory banks having identical addresses assigned thereto, identical data being written into said memory banks in response to a write command; and  
 25

a bank selection circuit for selecting one of said memory banks in response to a read command, and for sequentially selecting said memory banks in response to the write command such that said memory banks individually start a 30 write operation in a staggered manner.

7. The semiconductor memory device according to claim 6, wherein said bank selection circuit includes a shift register for sequentially activating bank selection signals for selecting the respective memory banks, in synchronism with the read command and the write command.  
 35

8. The semiconductor memory device according to claim 7, further comprising a write timing generator circuit for generating a write timing signal for executing the write operation, in response to the write command a number of times corresponding to the number of said memory banks, and  
 40

wherein during the write operation, said bank selection circuit sequentially activates the bank selection signals in synchronism with the write timing signal.  
 45

50

9. The semiconductor memory device according to claim 6, further comprising a data register for holding write data supplied in association with the write command, and  
 55

wherein the write data associated with a preceding write command and held by said data register is written into said memory banks in response to the write command.

10. The semiconductor memory device according to claim 9, further comprising:  
 5

an address register for holding a write address supplied in association with the write command;  
 an address comparator circuit for comparing, during the read operation, a read address supplied in association with the read command with the write address held by said address register, and outputting a coincidence signal if the read address coincides with the write address; and a data switching circuit, responsive to reception of the coincidence signal, for outputting, as readout data, the write data held by said data register.  
 15

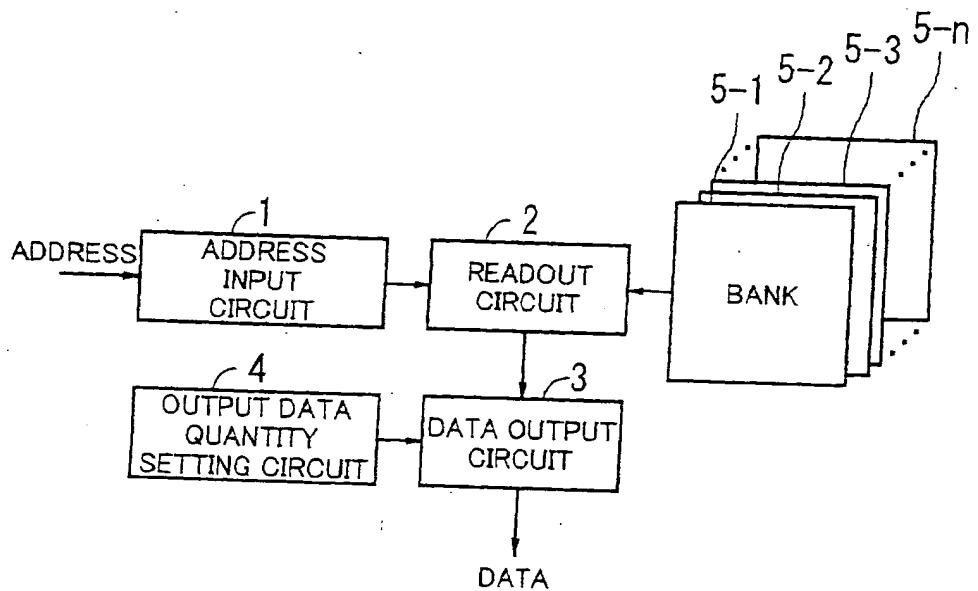
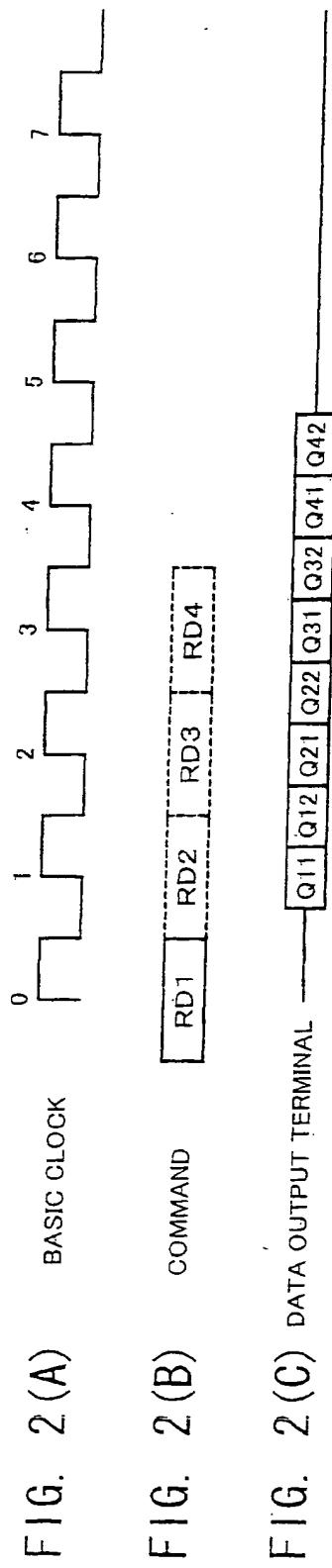


FIG. 1



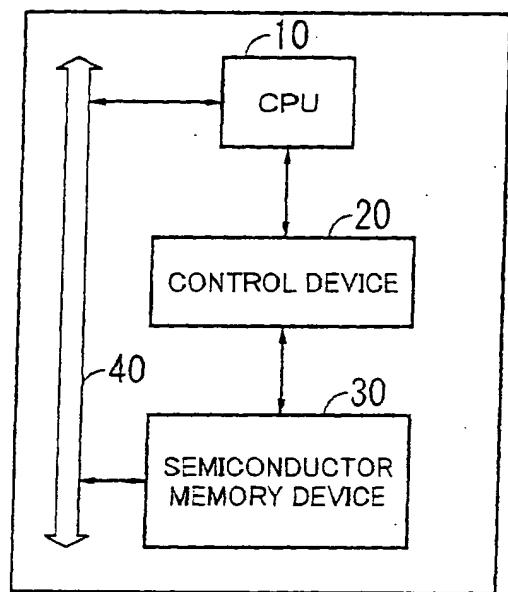


FIG. 3

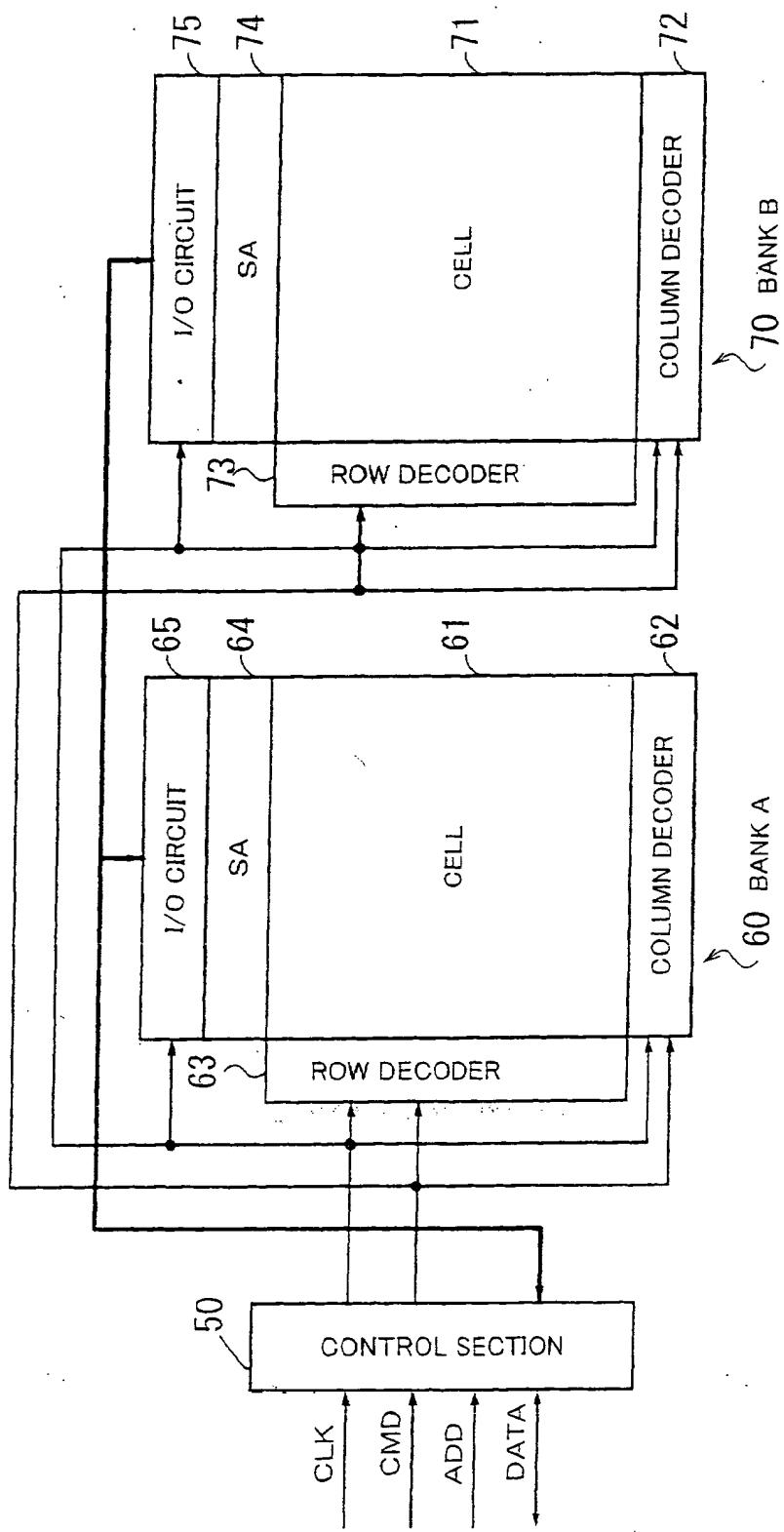


FIG. 4

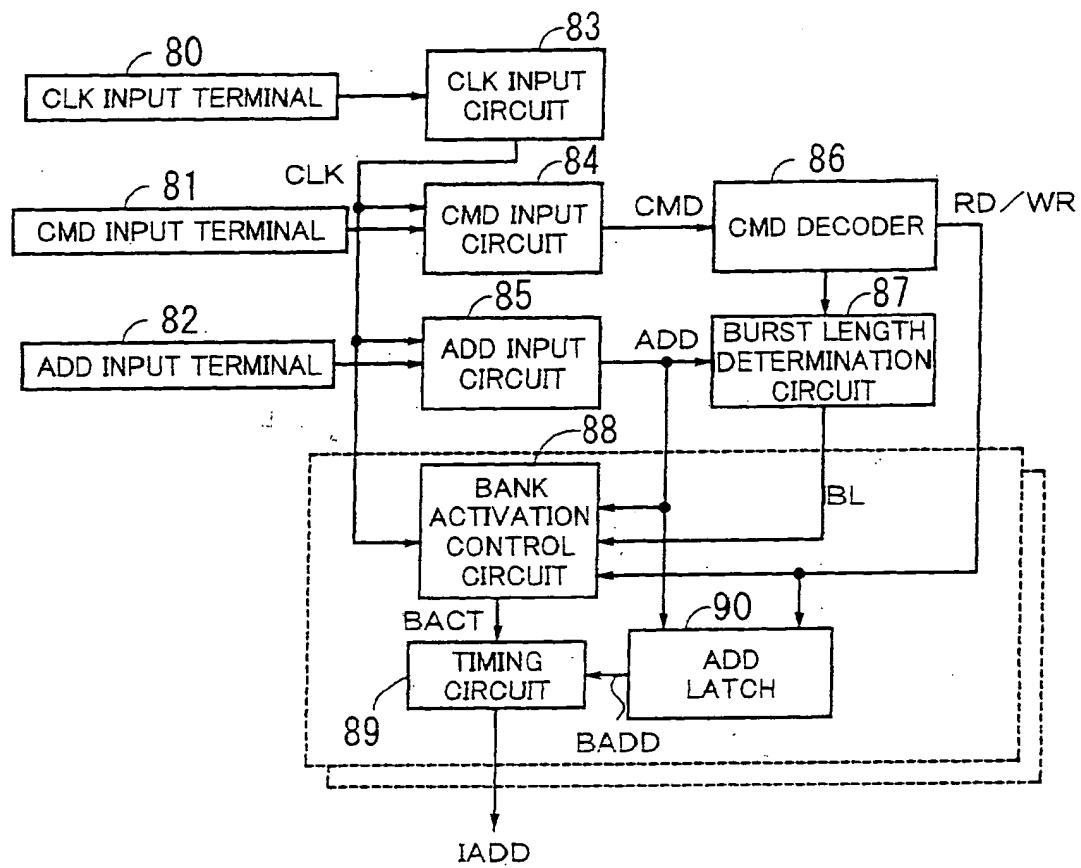


FIG. 5

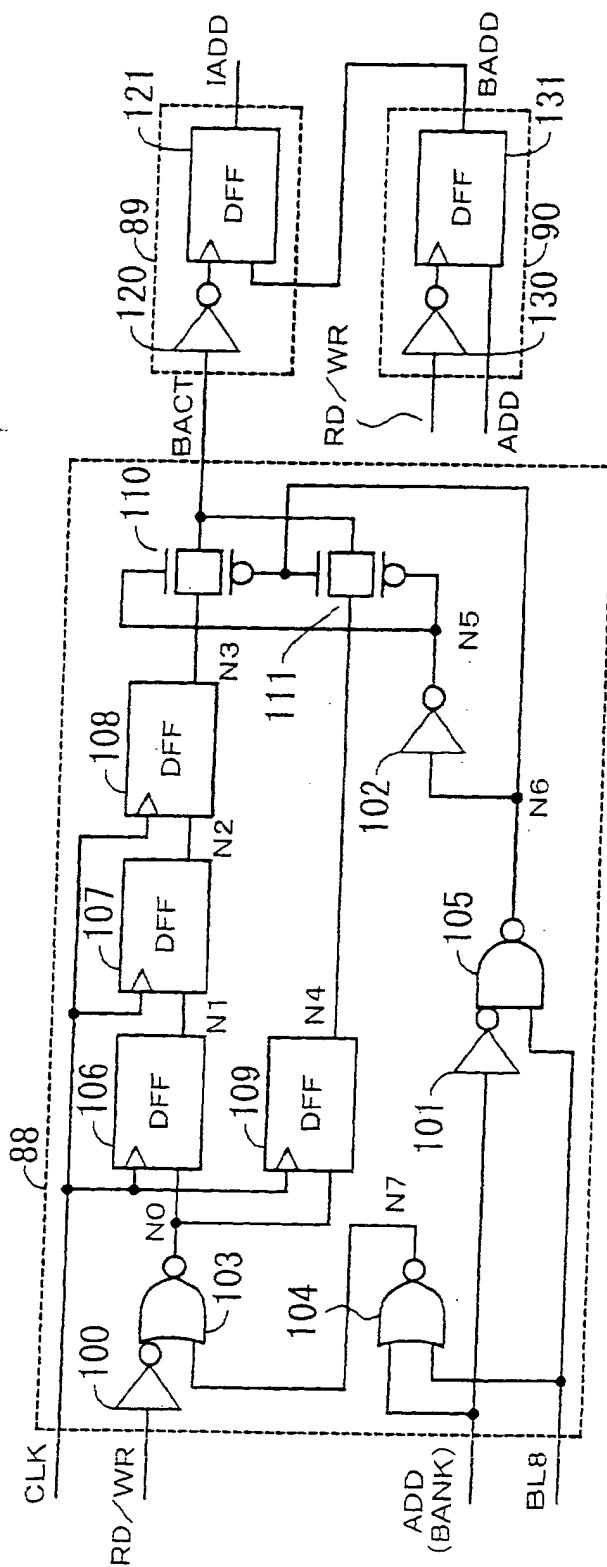


FIG. 6

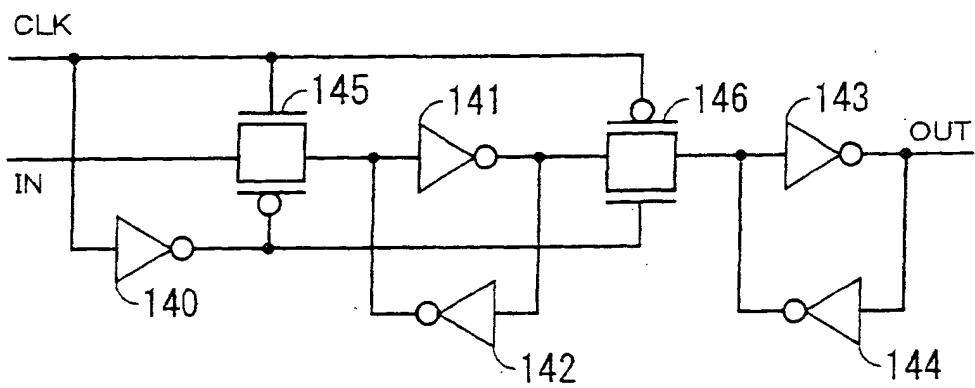


FIG. 7

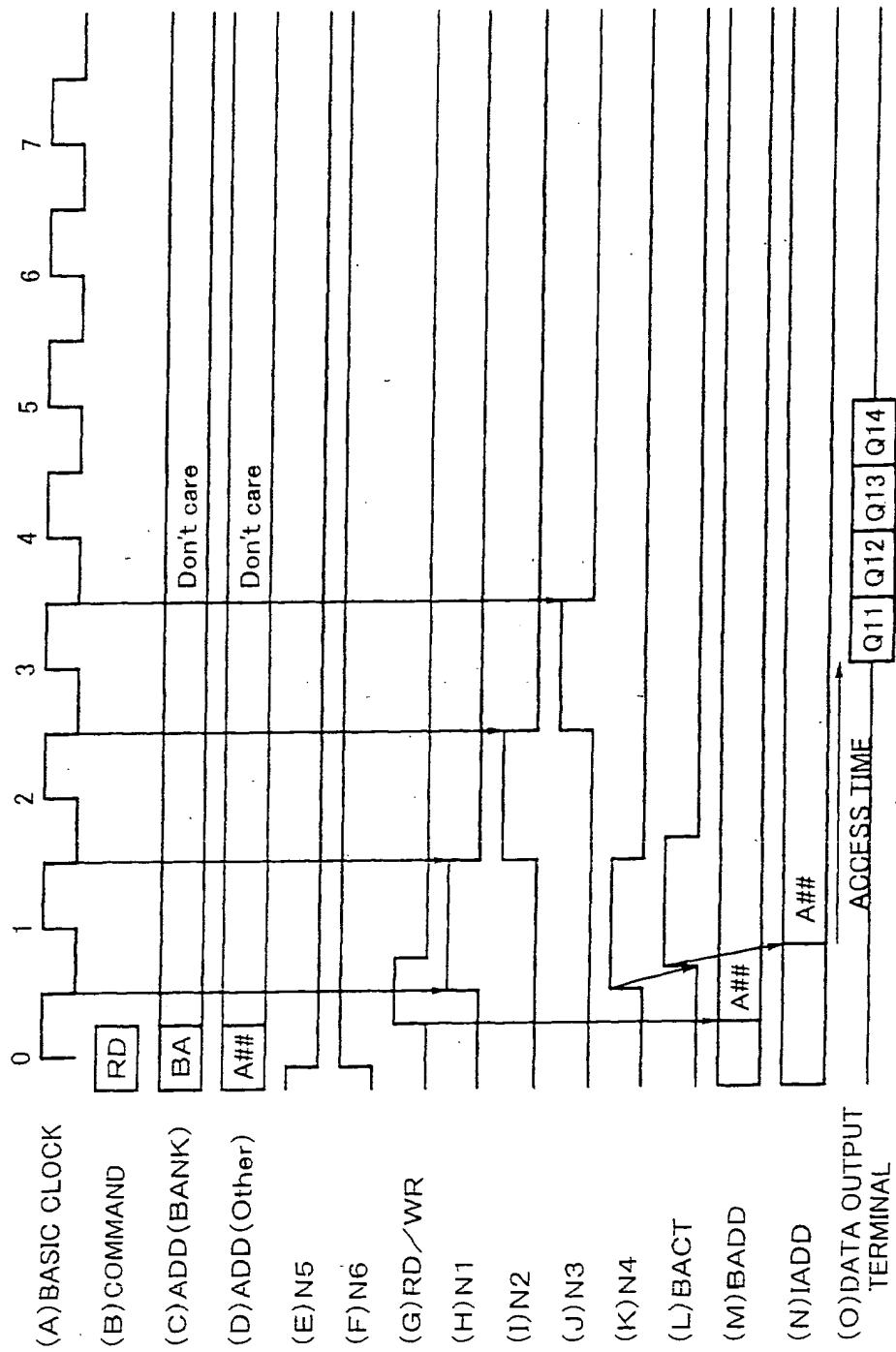


FIG. 8

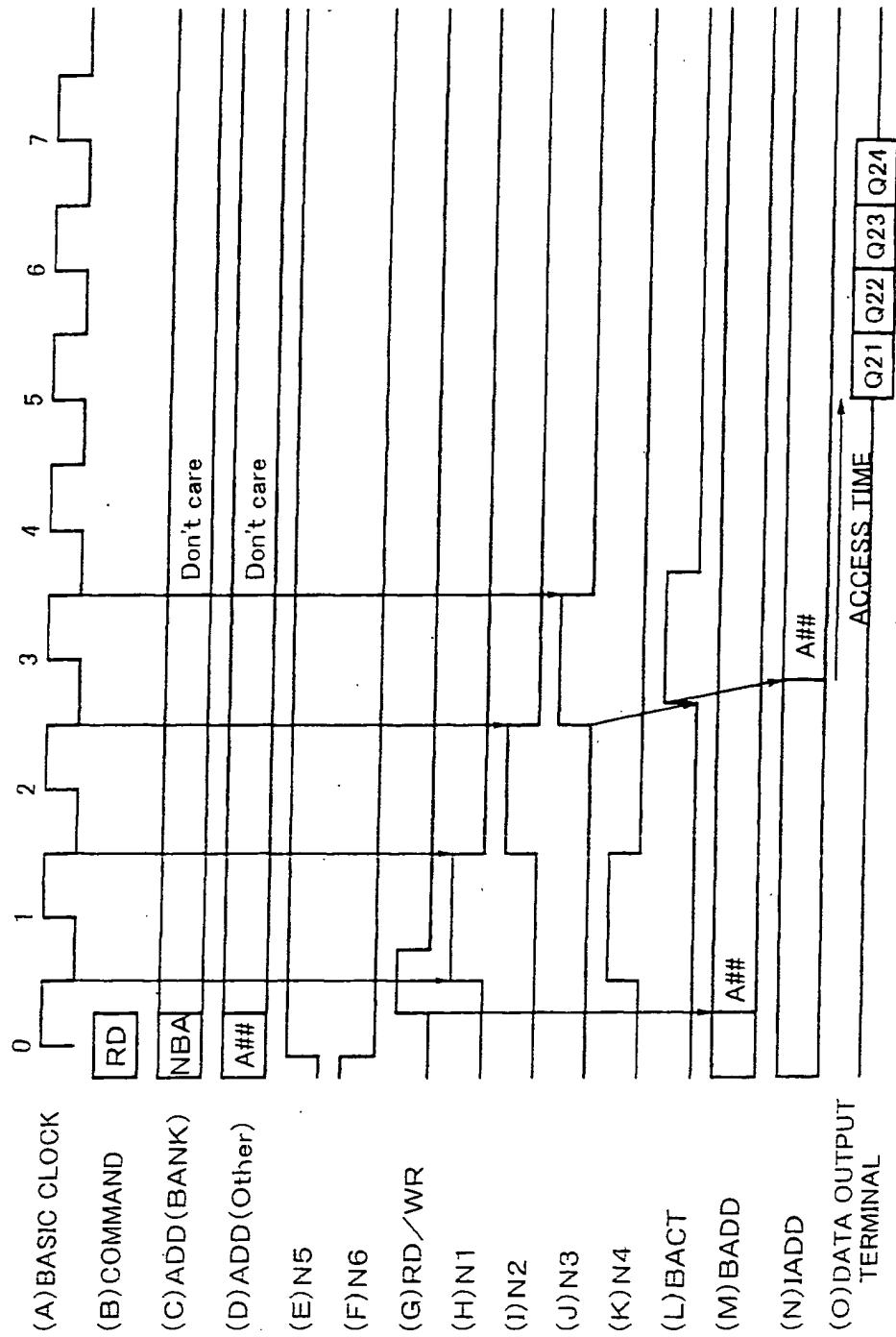


FIG. 9

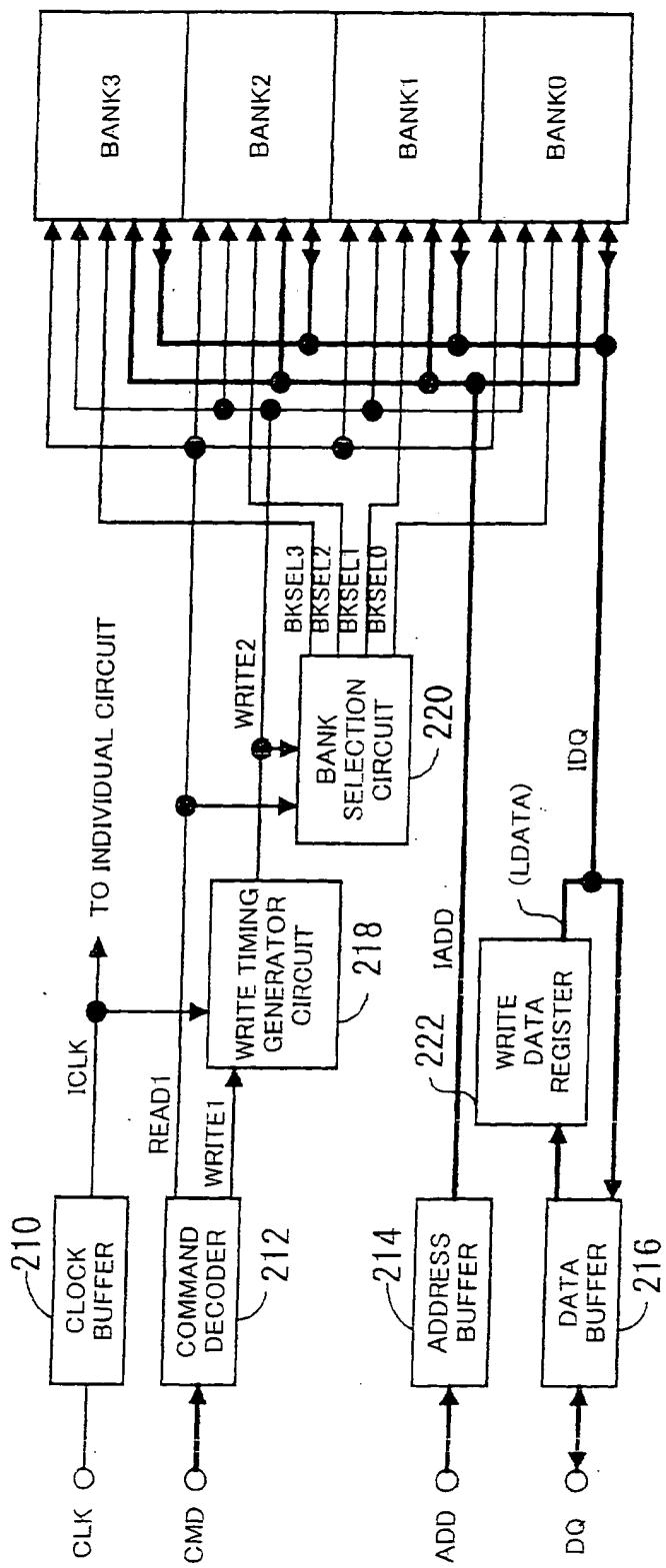


FIG. 10

BLOCK DIAGRAM SHOWING DETAILS OF BANK SELECTION CIRCUIT

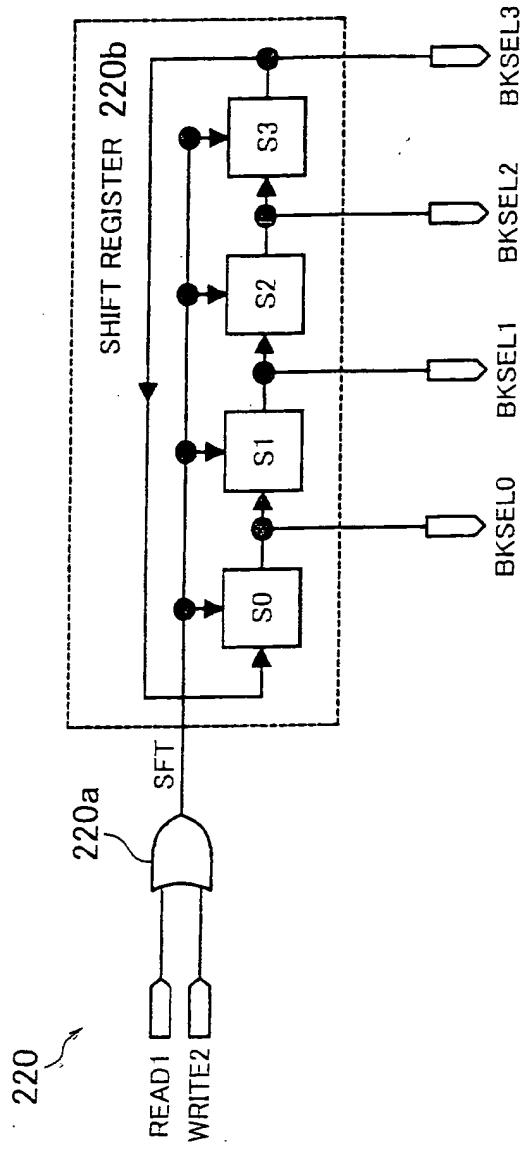


FIG. 11

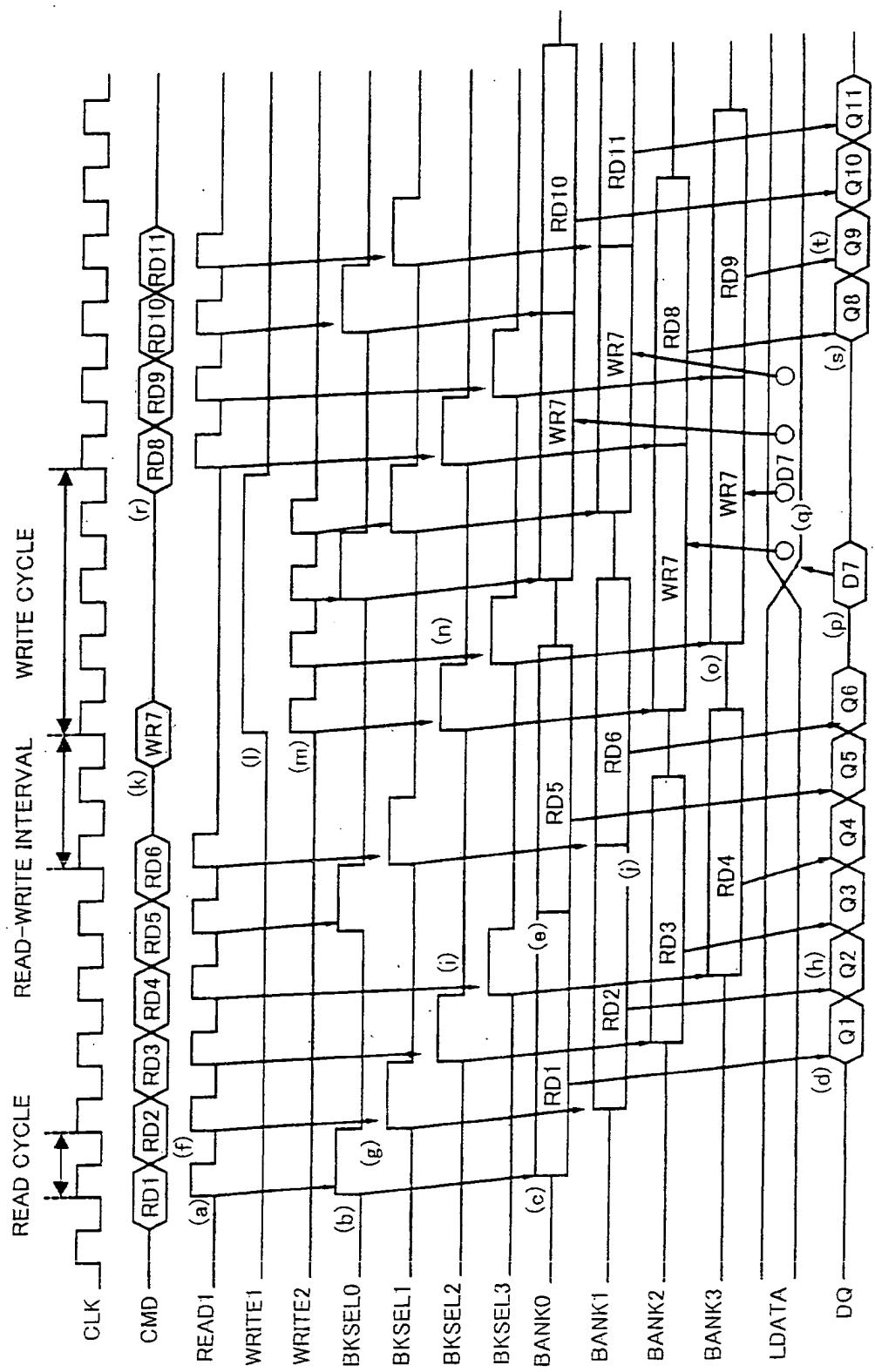


FIG. 12

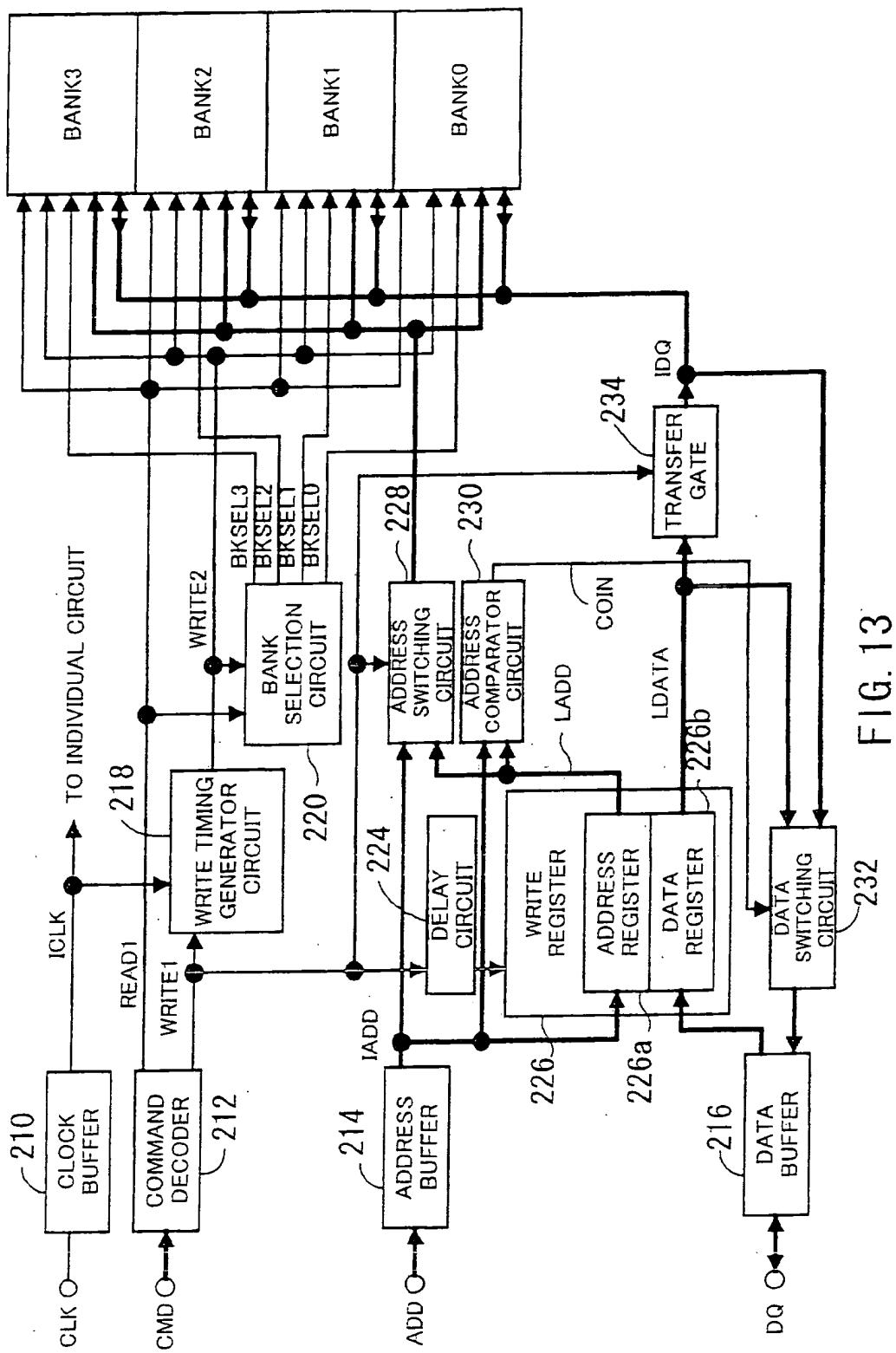


FIG. 13

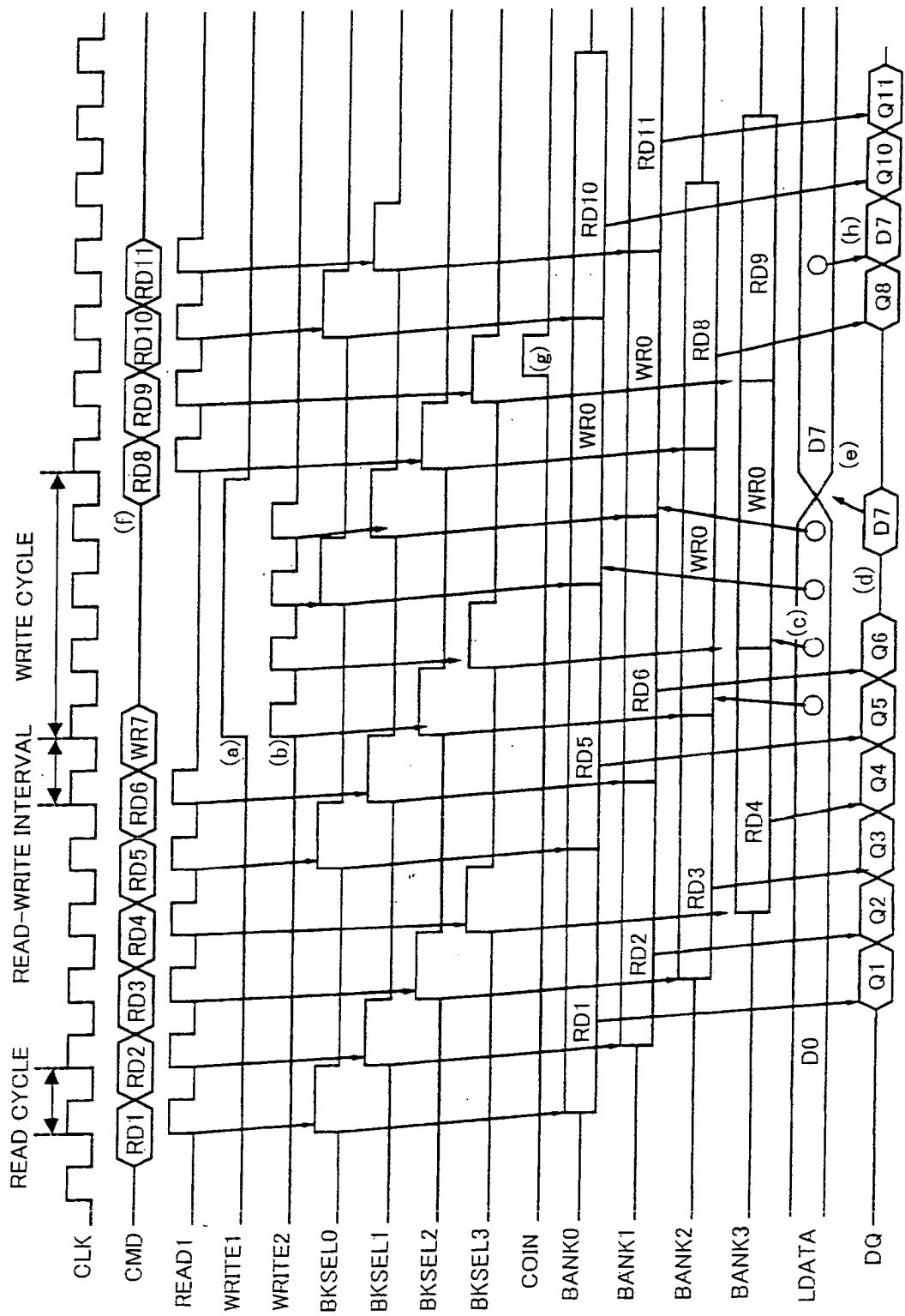


FIG. 14

FIG. 15 (A)  
PRIOR ART

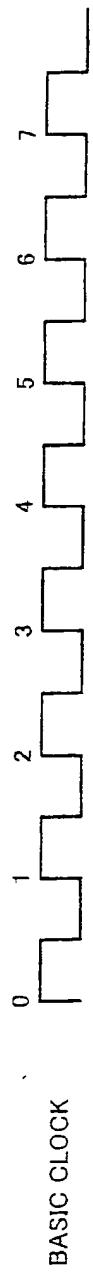


FIG. 15 (B)  
PRIOR ART

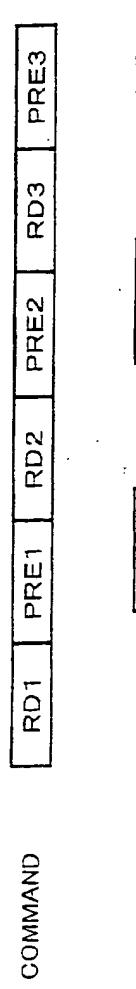


FIG. 15 (C)  
PRIOR ART



FIG. 16 (A)  
PRIOR ART

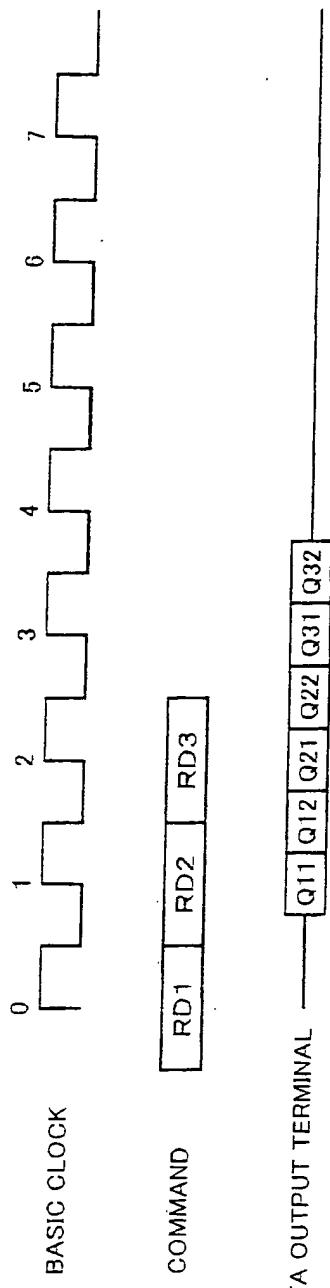


FIG. 16 (B)  
PRIOR ART

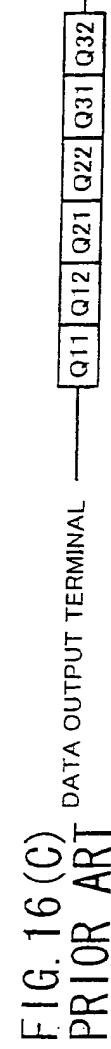


FIG. 17 (A)  
PRIOR ART

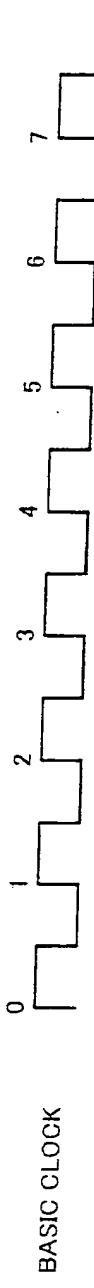
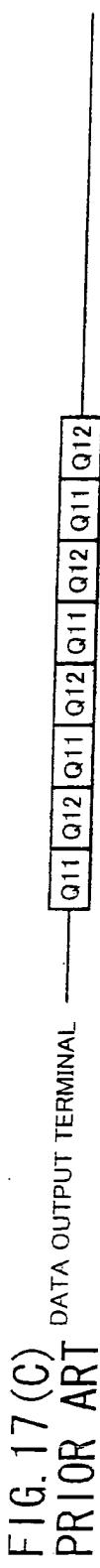
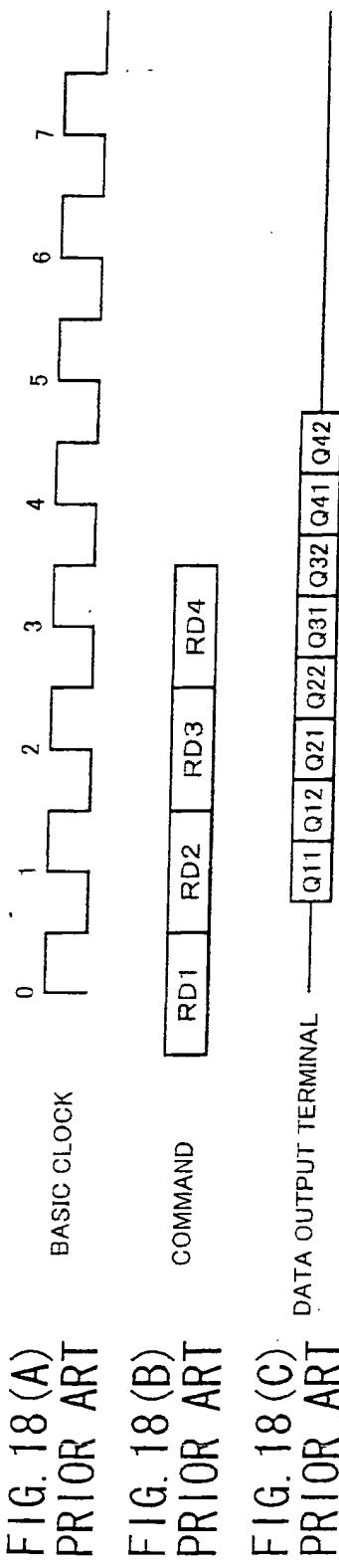


FIG. 17 (B)  
PRIOR ART



FIG. 17 (C)  
PRIOR ART





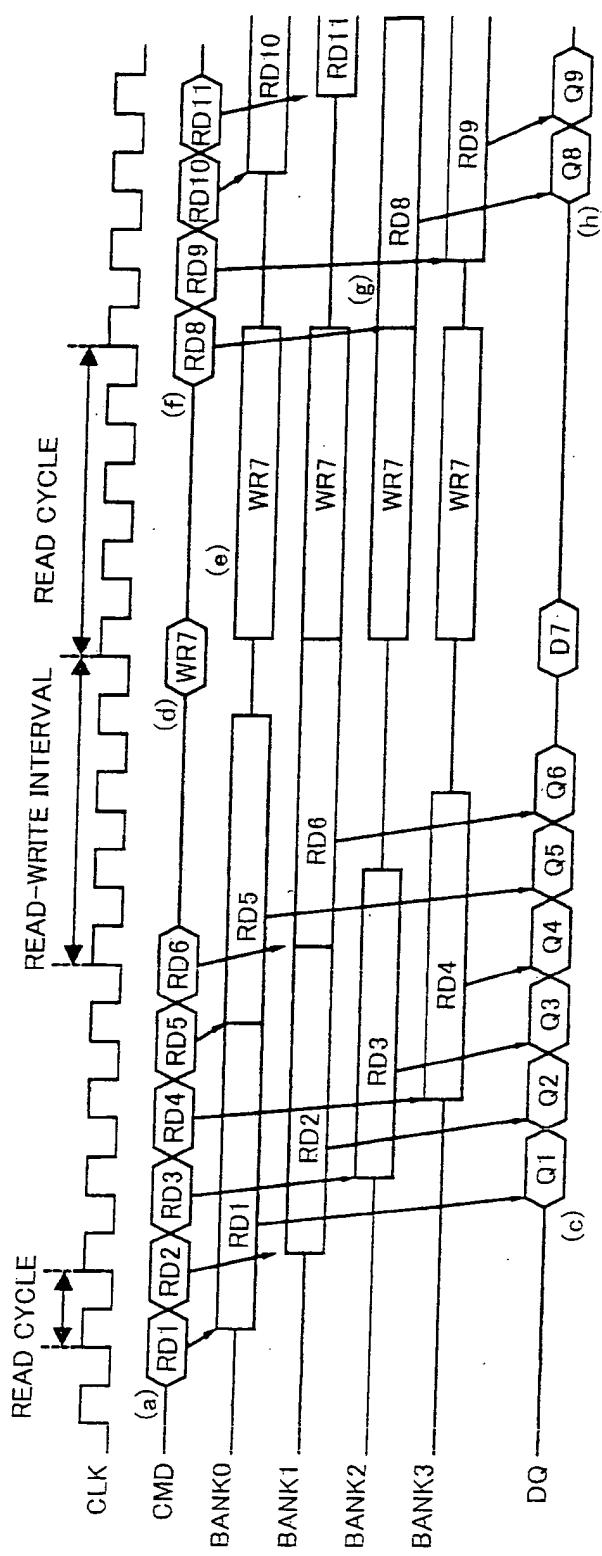


FIG. 19  
PRIOR ART